CLAIMS

What is claimed is:

1. A semiconductor package comprising:

a substrate including a core insulative layer with a central through hole, and a plurality of circuit patterns on a first surface of the core insulative layer, with each of the plurality of circuit patterns of the first surface including a ball land,

wherein a first subset of ball lands protrude further from the first surface than a second subset of the ball lands;

a plurality of same size solder balls, wherein a respective one of the solder balls is fused to each of the respective ball lands of the first and second subsets of the ball lands, whereby the solder balls fused to the ball lands of the first subset protrude further from the first surface than the solder balls fused to the ball lands of the second subset;

a semiconductor die disposed in the through hole and electrically coupled to the circuit patterns; and

a hardened encapsulant in the through hole covering the semiconductor die..

2. The semiconductor package of claim 1, wherein the core insulative layer includes a second surface opposite the first surface, said second surface being covered by a blanket conductive layer.

3. The semiconductor package of claim 1, wherein the core insulative layer includes a second surface opposite the first surface, said second surface being covered by a plurality of circuit patterns, with at least some of the circuit patterns of the second surface being electrically coupled through the core insulative layer to some of the circuit patterns of the first surface.

4. The semiconductor package of claim 4, wherein at least some of the circuit patterns of the second surface include a ball land.

5. The semiconductor package of claim 4, wherein a second semiconductor package is stacked thereon, said second semiconductor package including solder balls fused to the ball lands of the circuit patterns of the second surface.

6. The semiconductor package of claim 1, wherein the semiconductor die includes an active surface having a plurality of bond pads disposed near a perimeter of the active surface, and further comprising a monolithic slug affixed to the active surface of the semiconductor die within and without covering any of the bond pads, said slug being formed of a semiconductor material but not including any integrated circuits, and being fully covered by the encapsulant.

7. The semiconductor package of claim 6, wherein there are at least two of said slugs affixed to the active surface of the semiconductor die within and without covering any of the bond pads, said at least two slugs being fully covered by the encapsulant and spaced apart from each other.

8. The semiconductor package of claim 1, wherein the semiconductor die includes an active surface having a plurality of bond pads disposed near a perimeter of the active surface, and further comprising a monolithic slug affixed to the active surface of the semiconductor die within and without covering any of the bond pads, said slug being formed of metal and being fully covered by the encapsulant.

9. The semiconductor package of claim 8, wherein there are at least two said slugs affixed to the active surface of the semiconductor die within and without covering any of the bond pads, said at least two said slugs being fully covered by the encapsulant and being spaced apart from each other.

10. An electrical substrate comprising:

a core insulative layer having a first surface;

a layer of circuit patterns on the first surface, said circuit patterns each including one of a plurality of ball lands;

a plurality of same-size solder balls disposed in a plurality of rows, including a first row and a second row, said first row being closer to a perimeter of the core insulative layer than the second row, each said solder ball being fused to a respective one of the ball lands,

wherein the solder balls of the first row extend further from the first surface than the solder balls of the second row.

11. The electrical substrate of claim 10, wherein the core insulative layer includes a through hole between the first surface and an opposite second surface, and an encapsulated semiconductor die is disposed in the through hole.

12. The electrical substrate of claim 10, wherein a third row of the solder balls is disposed between the first row and the second row, and the solder balls of the third row extend further from the first surface than the solder balls of the second row.

13. The electrical substrate of claim 12, wherein the solder balls of the first row extend further from the first surface than the solder balls of the third row.

14. The electrical substrate of claim 10, wherein a third row of the solder balls is disposed between the first row and the second row, and the solder balls of the first row extend further from the first surface than the solder balls of the second and third rows.

15. The electrical substrate of claim 10, wherein the core insulative layer includes a second surface opposite the first surface, the second surface includes a plurality of circuit patterns, at least some of the circuit patterns of the second surface are electrically coupled through the substrate to some of the circuit patterns of the first surface, and some of the solder balls circuit patterns of the second surface include a ball land.

16. The electrical substrate of claim 10, wherein a semiconductor die is electrically coupled to at least some of the circuit patterns.

17. An electrical substrate comprising:

a core insulative layer having a first surface;

a layer of circuit patterns on the first surface, said circuit patterns each including one of a plurality of ball lands,

wherein a first subset of the circuit patterns include a stepped subportion including the ball land of the respective circuit pattern, and a second subset of the circuit patterns do not include a stepped portion, said stepped portion having a thickness from the first surface greater than a thickness of a remaining subportion of the respective circuit pattern.

18. The electrical substrate of claim 17, further comprising a plurality of solder balls, wherein a respective one of the solder balls is fused to the ball land of the circuit patterns of the first and second subsets.

19. The electrical substrate of claim 17, wherein the core insulative layer has a through hole extending between the first surface and an opposite second surface, and a semiconductor die and an encapsulant over the semiconductor die are disposed in the through hole.

20. The electrical substrate of claim 17, wherein a third subset of the circuit patterns also include a stepped subportion including the ball land of the respective circuit pattern, with the stepped subportion of the third set of circuit patterns having a thickness from the first surface of the substrate lesser than the thickness of the stepped subportion of the first subset of the circuit patterns.